

In the Claims

Please cancel claim 7.

The claims have been amended to read as follows:

1. (Amended) An ESD protection structure for use with an integrated circuit comprising:
 - a semiconductor substrate of a first conductivity type having a top surface;
 - a first well region of a second conductivity type disposed in the semiconductor substrate, the first well region having a center region, a side wall surface that contacts the top surface, and a bottom surface that contacts the side wall surface, the bottom surface under the center region contacting the substrate;
 - a second well region of the second conductivity type disposed in the semiconductor substrate;
 - a gap region of the first conductivity type disposed in the semiconductor substrate and separating the first well region from the second well region,
 - a first floating region of the second conductivity type disposed in the first well region adjacent to the gap region;
 - a second floating region of the second conductivity type disposed in the second well region adjacent to the gap region;
 - a first contact region of the first conductivity type disposed in the center region of the first well region and spaced apart from the first floating region;
 - a second contact region of the first conductivity type disposed in the second well region and spaced apart from the second floating region;
 - a first contact region of the second conductivity type disposed in the center region of the first well region and spaced apart from the first floating region; and
 - a second contact region of the second conductivity type disposed in the second well region and spaced apart from the second floating region.

SUBC!
Please add the following new claims:

--8. A device formed in a semiconductor material of a first conductivity type, the device comprising:

a first well of a second conductivity type formed in the semiconductor material, the first well having a dopant concentration;

a first contact region of the first conductivity type formed in the first well, the first contact region being electrically connected to a first node;

a second contact region of the second conductivity type formed in the first well, the second contact region being electrically connected to the first node;

a first trigger region of the second conductivity type formed in the first well, the first trigger region being spaced apart from the first and second contact regions;

a second well of the second conductivity type formed in the semiconductor material, the second well being spaced apart from the first well by a gap and having a dopant concentration;

a third contact region of the first conductivity type formed in the second well, the third contact region being electrically connected to a second node;

a fourth contact region of the second conductivity type formed in the second well, the fourth contact region being electrically connected to the second node; and

a second trigger region of the second conductivity type formed in the second well, the second trigger region being spaced apart from the third and fourth contact regions.

9. The device of claim 8 wherein

the first trigger region adjoins the semiconductor material; and
the second trigger region adjoins the semiconductor material.

10. The device of claim 9 wherein the first and second trigger regions are formed on opposite sides of the gap.

11. The device of claim 10 wherein

AMENDMENT IN RESPONSE TO
(OFFICE ACTION DATED DECEMBER 5, 2001)

the first trigger region has a dopant concentration greater than the dopant concentration of the first well; and

the second trigger region has a dopant concentration greater than the dopant concentration of the second well.

12. The device of claim 8 wherein

the first trigger region has a dopant concentration greater than the dopant concentration of the first well; and

the second trigger region has a dopant concentration greater than the dopant concentration of the second well.

13. The device of claim 8 wherein during a first ESD event, a first potential on the first node is greater than a second potential on the second node.

14. The device of claim 13 wherein during a second ESD event, a third potential on the second node is greater than a fourth potential on the first node.

15. The device of claim 8 wherein

the semiconductor material has a top surface;

the first well has a side surface that contacts the top surface, and a bottom surface that contacts the side surface; and

the first trigger region is spaced apart from the bottom surface.--